An Onboard Digital Transparent Processor for a Multi-beam Satellite

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Abstract – **This paper describes an efficient design of digital transparent processor payload subsystem, developed at Space Applications Centre (ISRO) for a multi-beam, high throughput communication satellite. The digital transparent processor, also called digital mesh processor, onboard a multi-beam communication satellite performs the functions of slicing the uplink bandwidth into fine granules, switching it as per user requirements and combining the bandwidth-granules for downlink transmission. It effectively serves as exchange-in-the-sky providing inter-beam and intra-beam connectivity among users in various spot beams; the connectivity may be unicast, multicast or broadcast. The digital transparent processor has four main subsystems namely Frequency Demultiplexer, Channel Switch, Frequency Multiplexer and Mesh Network Manager. A design verification model of the digital transparent processor has been implemented and its design, hardware and software implementation details, simulation and hardware performance results are presented.**

Keywords – **Digital transparent processor, digital mesh processor, transmultiplexer, onboard processing payload, Xilinx Virtex-5 FPGA.**

I. INTRODUCTION

Although there has been tremendous development in terrestrial fixed and wireless communications networks in recent years, satellites are still the optimum solution for broadcasting as well as multicasting and point-to-point communications, because of their coverage capability, limited ground infrastructure requirement, flexibility and easy last-mile connectivity. Multi-beam satellites are the order of the day, their development being driven primarily by the need to increase the satellite capacity. Multiple spot beams enable frequency reuse. Narrower spot beams entail increased EIRP and G/T, leading to smaller user terminals, even to the extent that handheld terminals are being used for communicating via a satellite.

Multiple spot beams necessitate the requirement of processor either on ground or onboard to provide connectivity among users spread across various beams. Conventional method has been to provide hub at ground to which all communication requests are routed, involving a double hop communication. Recently, a new type of digital payload based on the concept of transparent processing is emerging where inter-beam and intra-beam mesh connectivity to user terminals are provided onboard; thus forgoing the requirement of a hub earth station [1].

Conceptually a transparent processor works by performing segregation of uplink signals coming from receive spot beams using a filter-bank and switching them to designate transmit spot beams. Transformation of each frequency channel by the payload is linear time in-variant and there is no regeneration onboard. Fig. 1 shows the transparent processing concept.

An onboard transparent or mesh processor offers a number of compelling advantages like:

- Reduced transit time delay by half; thus giving better voice, video conference and interactive multimedia experience to the users.
- Allows the strategic users to adopt proprietary modulation and coding schemes; thus providing secure communication medium. The risk of cyber attacks or information leakage at hub is removed.
- The switchboard-in-the-sky provides a satellite communication system, which is not prone to risk of getting shut-down due to floods, fire, terrorist attacks or enemy bombing.
- Provides operational flexibility and deliver the needed capacity, coverage, connectivity and control in support of demanding operational scenarios.
- Saving of bandwidth required for hopping to hub.
- As hub is not required, the capital and operational expenditure for hub is saved. This can translate to cheaper services to users.
- The digital channelizer and beamformer, which provides the capability of multiple beamforming along with bandwidth routing, are often used in Mobile Satellite Services (MSS) applications where traffic dynamics are high and desired antenna performance invariably exceeds the capabilities of practically deployable analog multi-beam-antennas.

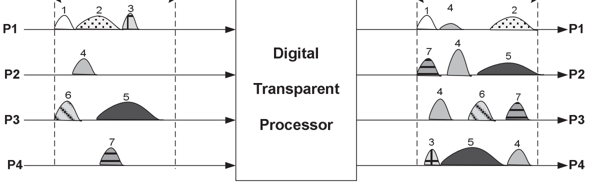


Fig. 1. Transparent Bandwidth Processing Concept

Implementation of the above described architecture with microwave components is limited in scope and functionality. Attempts to make scalable designs, processing entire transponder bandwidths may lead to payloads with very large mass and size. However the advent of space qualified digital processing elements, mainly FPGA, ASIC and memories has enabled the implementation of advanced digital signal processing concepts required for digital transparent processor in space with reasonable silicon footprint.

Of late, a few transparent processing payloads have been reported in the literature. Haardt, Herrero & Alagha [2] have described a design of a semi-transparent packet switch payload involving demodulation of only header part of data packet. Butash & Marshall [3] have described an architecture of a digital channelizer for multi-beam payloads. This paper describes an efficient design of transparent processor, developed at Space Applications Centre (ISRO) for a multi-beam, high throughput satellite, along with details of hardware implementation using Xilinx FPGAs. The developed model features:

- A modular and expandable frequency demultiplexer, designed in an iterative flow, using a set of objective functions, to optimize complexity and performance
- A novel non-blocking time-space switch design, based on multiple ping-pong dual port RAMs
- A modular and expandable frequency multiplexer design with computationally efficient digital frequency up conversion
- A mesh network manager, which does on-demand bandwidth allocation to user terminals and maintains onboard terminal and bandwidth allocation database

This paper is organized as follows. Section II describes requirements and specifications. Section III describes the system design. Section IV describes the sub-system specifications, design and implementation details. Section V gives the simulation and hardware (design verification model) results.

II. REQUIREMENTS AND SPECIFICATIONS

The transparent processor developed at Space Applications Centre (ISRO) is envisaged for a Ku/Ka band satellite with 16 Ku-band user beams, covering entire India and two Ka-band hub beams. The frequency plan of the satellite employs frequency and polarization re-use in spatially separated Ku-band user beams for efficient spectrum utilization. Out of total available bandwidth of 125 MHz per user beam, 15.625 MHz is assumed to be allocated for transparent processing and rest for the conventional bent pipe payload.

The transparent processor slices the 15.625 MHz uplink bandwidth of each beam into 16 small concatenatble granules of 976 KHz. These granules are switched as per the request received from the user terminals or from telecommand. Finally it combines the 16 granules into a single signal for each beam for downlink transmission.

TABLE 1: SYSTEM SPECIFICATIONS

	Parameter	Specification
	Input specifications:	
1.	Input ports	8
2.	Beams / input port	2
3.	Bandwidth / input port	31.25 MHz
	Channelization specifications:	
4.	Bandwidth granularity	976 KHz
5.	Channelization	In multiple (1,2,..,16) of bandwidth granularity
6.	Guard band	1 granule
	Switch specifications:	
7.	Cross-port connections	256 x 256
8.	Switch configuration	On-demand allocation: by user request Permanent allocation: by telecommand
9.	Switching options	unicast, multicast, broadcast
10.	Channel gain	-7 to 7 dB (programmable in 1 dB step)
	Output specifications:	
11.	Output ports	8
12.	Beams / output port	2
13.	Bandwidth / output port	31.25 MHz

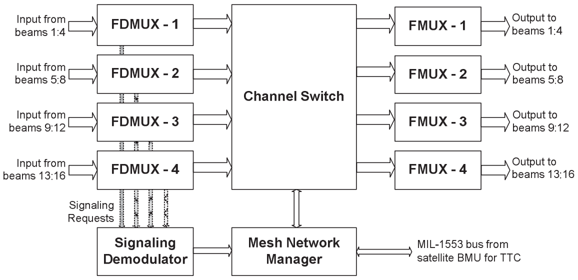


Fig. 2. Transparent Processor Payload Architecture

The payload also provides resource management functions. The database of bandwidth connectivity is maintained onboard, which is updated in real time by user requests for bandwidth allocation/de-allocations. Reservation of bandwidth for long term or strategic customers may be made by network control centre through telecommand. The database of user terminals is maintained onboard, which is updated by network control centre through telecommand.

The main specifications of the Digital Transparent Processor are given in table-1.

III. SYSTEM DESIGN

A schematic representation of the transparent processor architecture is shown in fig. 2.

The transparent processor comprises of four main constituents namely the Frequency Demultiplexer (FDMUX) cards for slicing the input signal in small granules, Channel Switch card for programmable connectivity between input and output, Frequency

Multiplexer (FMUX) card for combining individual granules to form a single signal for downlink transmission and mesh network manager (MNM) card for processing the signaling requests from individual terminals and telecommands and also performing usual network manger operations like terminal database management, bandwidth allocation management, network usage logging etc. Each FDMUX and FMUX card processes four beams, hence total four cards of each are required to process 16 beams.

The design of transparent processor is based on near perfect reconstruction filter bank theory well documented in literature [4][5]. The analysis and synthesis filters are derived by cosine modulation of a low pass prototype filter, $p_0(n)$. Hence, the performance of the filter bank depends on the design of prototype filter. The analysis filters $h_k(n)$ and synthesis filters $f_k(n)$ for an M-channel transmultiplexer are given in equation (1) below.

$$h_k(n) = 2p_0(n)\cos\left(\frac{\pi}{2M}(2k+1)\left(n-\frac{N}{2}\right)+\theta_k\right)$$

$$f_k(n) = 2p_0(n)\cos\left(\frac{\pi}{2M}(2k+1)\left(n-\frac{N}{2}\right)-\theta_k\right) \qquad (1)$$

$$\theta_k = (-1)^k \frac{\pi}{4}$$

$$k = 0,\ldots M-1$$

N=Prototype filter order (essentially even)

IV. DESIGN AND IMPLEMENTATION

The design and implementation considerations and details for the four types of cards are provided into below subsections.

A. Frequency Demultiplexer (FDMUX)

The FDMUX card accomplishes the task of beam segregation and beam channelization for four beams. Fig. 3 shows the design approach of the card.

The FDMUX card receives four beams as two dual-beams, with each dual-beam occupying 31.25 MHz bandwidth. These are sampled by two ADCs at 125 MHz; enough to take care of guard band and input SAW filter design. Each dual-beam signal feeds to 4-channel frequency demultiplexer module, which separates two beams out of dual-beam. The separated beams are further processed by second filter bank, to segregate each beam into sixteen channels each of bandwidth 976 KHz. Thus a FDMUX card outputs 64 channels from four beams, which are digitally multiplexed, serialized and sent to the channel switch card. The entire processing is done in two Xilinx Virtex-5 FPGAs.

The design of 4-channel frequency demultiplexer module is based on cosine modulated filter bank, derived from a low pass prototype filter [6]. It can be represented as (2) with M=4.

$$Y_i(z) = \frac{1}{M}\sum_{k=0}^{M-1} H_i\left(z^{1/M}W^k\right)X\left(z^{1/M}W^k\right) \qquad (2)$$

$$W = e^{-j2\pi/M}$$

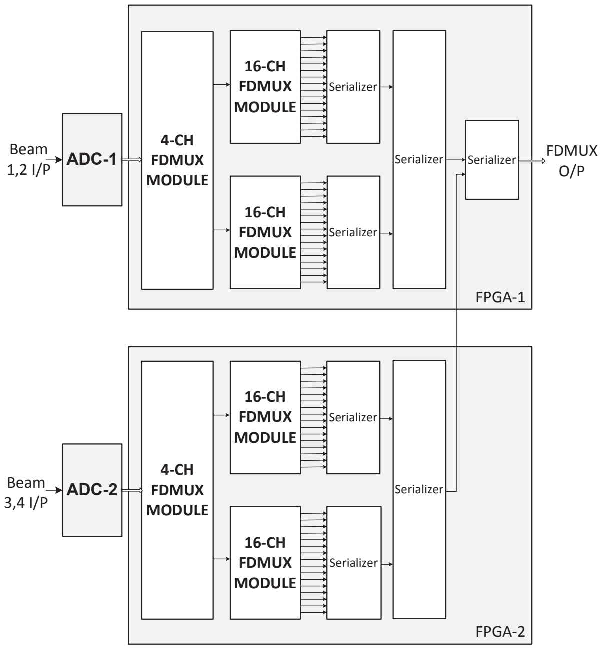


Fig. 3. Frequency Demultiplexer Card Design

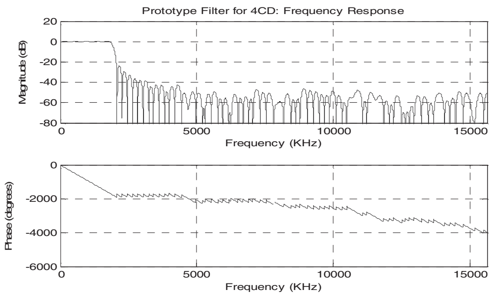


Fig. 4. 4-Channel Frequency Demultiplexer Prototype Filter Response

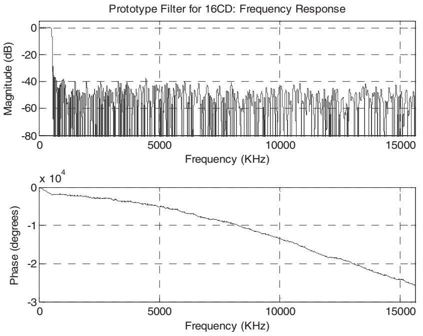


Fig. 5. 16-Channel Frequency Demultiplexer Prototype Filter Response

where,	$X(z)$,	z-transform of the input
	$Y_i(z)$,	z-transform of i^{th} output
	$H_i(z)$,	modulated filter in the i^{th} branch
	M ,	no. of outputs/ decimation rate
	i =	0,1,...,M-1

A 161-tap prototype filter is used for 4-channel frequency demultiplexer. The prototype filter is designed with Kaiser window (β = 1). The frequency response of the prototype filter is shown in fig. 4. This filter provides channel granularity of 15.625 MHz, passband ripple of 0.1 dB (peak) and cross beam isolation of 28.4 dB (min).

The design of 16-channel frequency demultiplexer module is also based on cosine modulated filter bank, derived from a low pass prototype filter. It can be represented as (2) with M=16. A 641-tap prototype filter is used for 16-channel frequency demultiplexer. The prototype filter is designed with Kaiser window (β = 2.05). The frequency response of the prototype filter is shown in fig. 5. This filter provides channel granularity of 976 KHz, passband ripple of 0.66 dB (peak) and cross channel isolation of 38.37 dB (min).

B. Channel Switch

The design of channel switch is based on the concept of a time-space switch matrix [7]. It performs the function of switching any of the total 256 input channels to any of the total 256 output channels, as per the instruction received from the mesh network manager. In essence, it is a 256 x 256 switch-in-the-sky. Fig. 6 shows the schematic design of the channel switch, implemented using a single Xilinx Virtex-5 FPGA.

The channel switch uses a novel design approach of time-space switch. This time-space switch is a scalable two-stage combinational switch, which uses multiple ping-pong dual port random access memories (DPRAM) for implementing the non-blocking time-space switch. This non-blocking time-space switch accepts time multiplexed data and images it simultaneously in plurality of DPRAMs. These multiple images allow the switch to route all incoming channels to any output channel without any blocking limitation. As it uses output controlled switch, it also provides functionality of multicast and broadcast. The channel switch can also provide programmable gain to individual output channel. The switched outputs are sent to frequency multiplexers which form final IF outputs.

C. Frequency Multiplexer (FMUX)

The FMUX card implements the inverse function of the FDMUX card. Fig. 7 shows the design of FMUX card.

The FMUX receives 64 channels, each of 976 KHz bandwidth, corresponding to 4 beams from the channel switch in TDM form. These 64 channels are deserialized to separate 16 channels corresponding to each of four beams. The 16 channels for each beam are fed into a 16-channel frequency multiplexer module, which combines the sixteen channels by frequency-shifting and filtering, to output a single signal containing all the sixteen channels in FDM form, occupying total 15.625 MHz bandwidth.

The transformation by 16-channel frequency multiplexer module can be expressed as:

$$Y(z) = \sum_{i=0}^{L-1} X_i\left(z^L\right) F_i(z) \tag{3}$$

where, $Y(z)$, z- transform of output signal
$X_i(z)$, z-transform of i^{th} channel input signal
$F_i(z)$, filter for the i^{th} channel
L, no. of channels = 16

Next, digital frequency up-converters (DFUC) efficiently translate each beam signal to a higher frequency band by selecting a replica from poly-phase interpolation and applying spectral inversion wherever needed. The up-converted signals for beam 1 & 2 as well as for beam 3 and 4 are combined to form two dual-beams. The final signal is again efficiently up-converted to the required band by polyphase interpolation. In end, a pre-emphasis filter is applied to compensate for DAC sinc roll-off [8].

The design has been implemented in two Xilinx Virtex-5 FPGAs and two Digital to Analog converters.

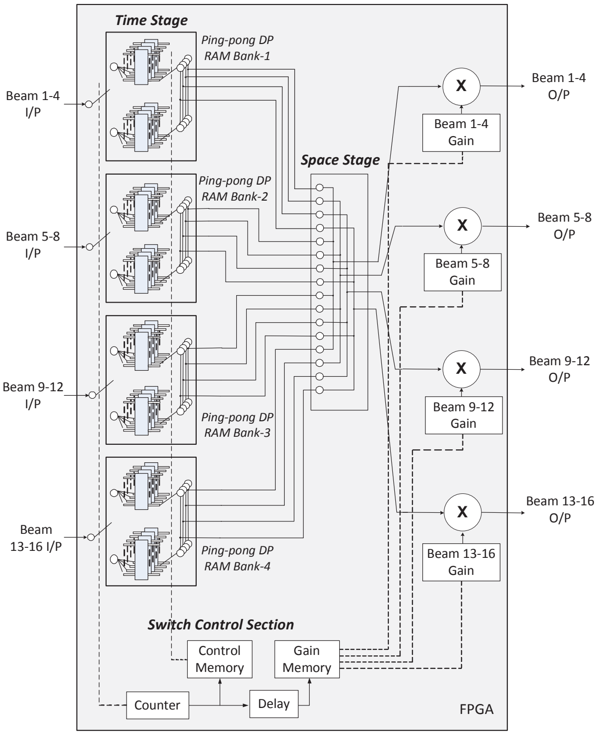


Fig. 6. Channel Switch Card Design

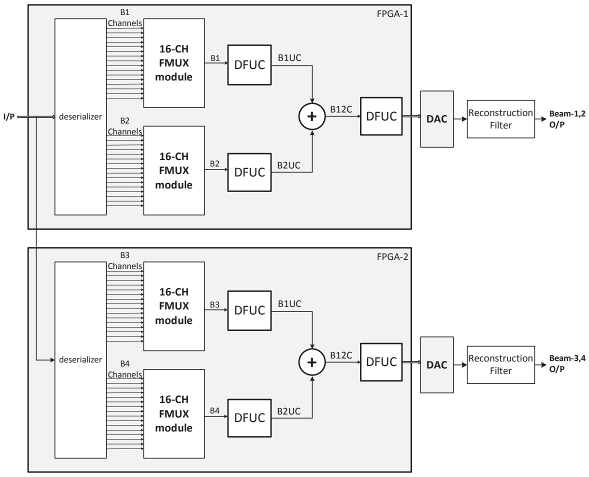


Fig. 7. Frequency Multiplexer Card Design

D. Mesh Network Manager

The Mesh Network Manger (MNM) performs the function of Network Management System for the users of the satcom network. It interfaces with signaling chain to receive the channel allocation requests from individual terminals. Based on signaling request and priority assignments, it allocates the bandwidth to the users and acknowledges to them. It programs the channel switch to make proper connection, over which the users can communicate. After the communication is over, the user terminals would request for de-allocation of the bandwidth, upon which, the mesh processor frees the bandwidth.

Fig. 8 shows the architecture of MNM card. The card is based on 80196 micro-controller and Actel RTAX250 FPGA.

The mesh network manger maintains the database of frequency allocations and commissioned terminals. The network usage information is transmitted on the TDM downlink as well as in telemetry, which can be used for monitoring the network and generating billing information.

The mesh network manger has a MIL-STD-1553B interface to spacecraft to receive telecommands and transmit telemetry. The network control centre can also issue channel allocation telecommands as well as receive bandwidth allocation information.

E. Implementation Details

Fig. 9 shows the design verification model of Digital Transparent Processor.

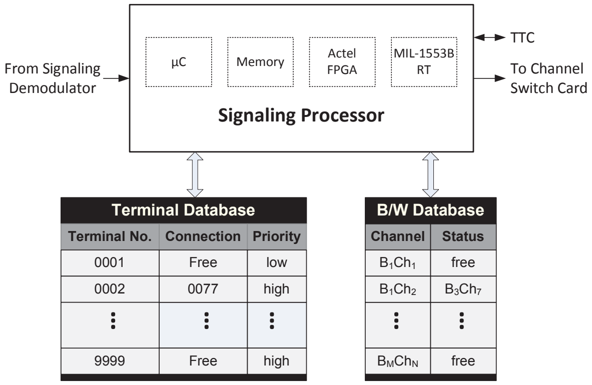
Table-II gives the resource utilization factors for each card. It may be noted that the logic utilization ratio is constrained by high clock rate of 250 MHz in frequency multiplexer card and frequency demultiplexer card.

V. SIMULATION AND HARDWARE TEST RESULTS

The design of the transparent processor was simulated in a MATLAB/Simulink environment to verify the algorithm, optimize the prototype filter design and quantify the extent of quantization errors on the algorithm performance.

Fig. 10 shows the methodology of simulation for digital transparent processor. Table-III shows the simulation results. Fig. 11 shows the Error Vector Magnitude (EVM) performance at different SNR.

Table-IV shows the hardware test results for narrowband and wideband input signals with unicast, broadcast and multi-cast switching.



Terminal Database

Terminal No.	Connection	Priority
0001	Free	low
0002	0077	high
⋮	⋮	⋮
9999	Free	high

B/W Database

Channel	Status
B_1Ch_1	free
B_1Ch_2	B_3Ch_7
⋮	⋮
B_MCh_N	free

Fig. 8. Architecture of Mesh Network Manager Card

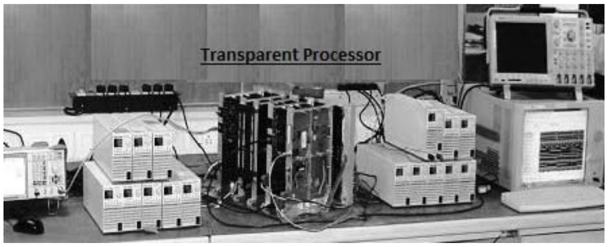


Fig. 9. Integrated Transparent Processor and Test Setup

TABLE II: HARDWARE RESOURCES UTILIZATION

Card	Device	Utilization Factor
Frequency Demultiplexer	FPGA-1 (Xilinx V5)	36% (logic), 7% (I/O)
	FPGA-2 (Xilinx V5)	36% (logic), 7% (I/O)
Channel Switch	FPGA (Xilinx V5)	6% (logic), 60% (I/O)
Frequency Multiplexer	FPGA-1 (Xilinx V5)	41% (logic), 10% (I/O)
	FPGA-2 (Xilinx V5)	41% (logic), 10% (I/O)
Mesh Network Manager	Micro-controller 80196	32% (loading)
	FPGA(Actel RTAX250)	21% (logic), 62% (I/O)

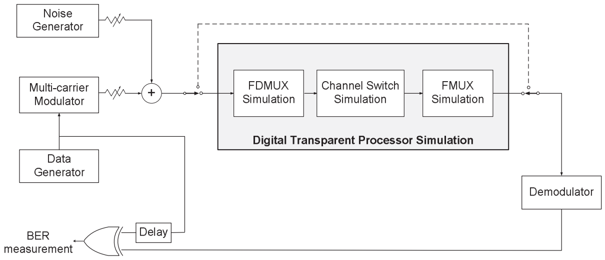


Fig. 10. Transparent Processor Simulation Model

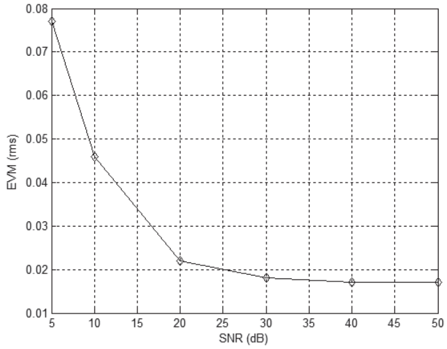


Fig. 11. EVM performance of the digital transparent processor

TABLE III: SIMULATION RESULTS

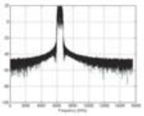
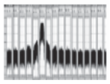
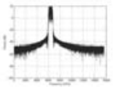
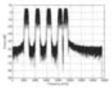
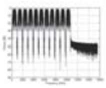
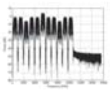
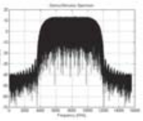
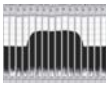
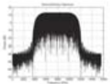
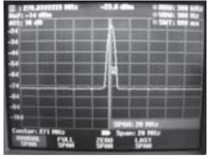
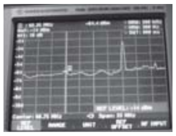
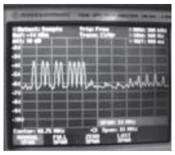
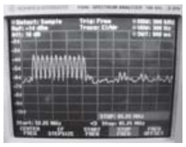
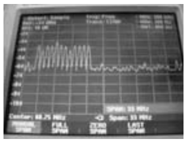
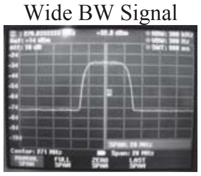
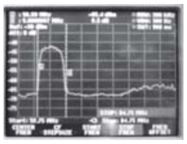
Input	Operational Mode	Simulation Results	
		FDMUX O/P	TP O/P
Narrow BW signal 	Unicast		
	Multicast		
	Broadcast		
	Broadcast with downlink power control		
Wide BW signal 	Unicast		

TABLE IV: HARDWARE RESULTS

Input	Operational Mode	TP O/P
Narrow BW signal 	Unicast	
	Multicast	
	Broadcast	
	Broadcast with downlink power control	
Wide BW Signal 	Unicast	

VI. CONCLUSION

This paper describes the architecture, algorithms and implementation details of a proof of concept model of a digital transparent processor developed at Space Applications Centre (ISRO) for future multi-beam satellites.

The transparency is an important feature as it ensures future compatibility with regard to future evolution of markets and standards. The transparent processor being developed offers flexibility to service providers in beam channelization and switching and allows meshed network with multicast and broadcast options. The bandwidth to the users is made available on-demand basis. Thus it essentially serves as an exchange-in-the-sky and provides hubless mesh connectivity.

Simulation and hardware test results are presented, which show the operations of the transparent processor with on-demand connectivity and telecommand controlled connectivity in unicast, multi-cast and broadcast modes with downlink power control.

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